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Nonvolatile polycrystalline silicon thin-film-transistor memory with oxide/nitride/oxide stack gate dielectrics and nanowire channels

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In this work, the authors study a polycrystalline silicon thin-film transistor (poly-Si TFT) with oxide/nitride/oxide (ONO) stack gate dielectrics and multiple nanowire channels for the applications of both nonvolatile silicon-oxide-nitride-oxide-silicon (SONOS) memory and switch transistor. The proposed device named as nanowire SONOS-TFT has superior electrical characteristics of a transistor such as on/off current ratio, threshold voltage (V_{th}), and subthreshold slope due to the good gate control ability originated from fringing electrical field effects. Moreover, the proposed device under adequate operation scheme can exhibit high program/erase efficiency and good retention time characteristics at high temperature. © *2007 American Institute of Physics*.
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Polysilicon thin-film transistors (poly-Si TFTs) are widely used to integrate driver circuits for active-matrix liquid-crystal displays due to its high field effect mobility and driving current.[1,2] In addition, the further improvement of poly-Si TFT performances can enable various functional devices, such as memory and controller, to be integrated on a glass panel to achieve system-on-panel (SOP) display.[3–6] The low-power consumption is the first priority requirement for SOP applications. It is well known that the nonvolatile memory is utilized extensively in various portable electronic systems because of its attributes of low-power consumption and nonvolatility. The conventional nonvolatile memory with floating-gate structure faces a limit due to its complicated fabrication process for integration on a display panel. As a result, the silicon-oxide-nitride-oxide-silicon (SONOS)-type memory has become a promising candidate for SOP application due to its full process compatibility. Nevertheless, several issues on performance and reliability such as insufficient programing/erasing efficiency, poor endurance, and short retention time must be overcome.[7,8] Recently, SONOS-type poly-Si TFT fabricated by sequential lateral solidifica-

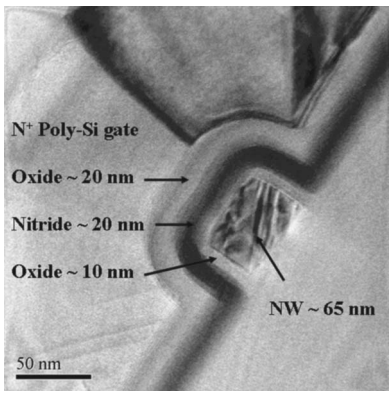

FIG. 1. TEM micrograph of a single nanowire channel of the NW SONOS-TFT.

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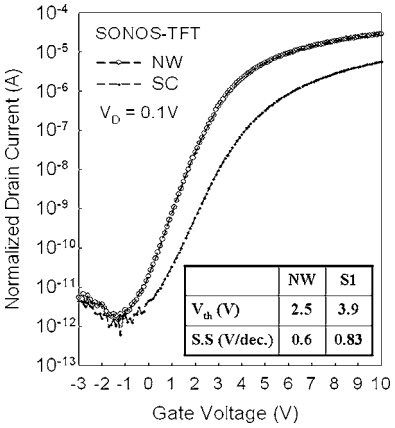

FIG. 2. Comparison of I_D-V_G transfer characteristics of the SC and the NW SONOS-TFTs.

tion is reported to improve the programing/erasing efficiency due to field-enhanced tunneling at the Si protrusions of grain boundaries.[9] However, the variation of the location of poly-Si grain boundaries by laser recrystallization method may still be a concern.

Based on our previous study,[10,11] the poly-Si TFT with nanowire channels can exhibit good gate control. Thus, poly-Si TFT combined with both SONOS memory and nanowire channels, named as nanowire (NW) SONOS-TFT, is proposed for the application of high performance transistor and high program/erase (PE) efficiency nonvolatile memory device.

In this work, the SONOS-TFT with a multiple NW structure composed of ten strips of 65 nm nanowire channel was proposed, and the device with a single channel (SC) structure with $W=1$ μm was also fabricated for comparison. Silicon wafers with a 400 nm thermal oxide were used as the starting substrate. An undoped amorphous silicon (*a*-Si) layer with thickness of 500 nm was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C. The deposited *a*-Si layer was then recrystallized by solid-phase crystallization at 600 °C for 24 h in nitrogen ambient. Then the device active region was patterned by electron beam lithography and transferred by reactive ion etching. After the active region was defined, a 50-nm-thick oxide/nitride/oxide (ONO) multilayer gate dielectric with a bottom tetraethyl-*ortho*-silicate (TEOS) oxide (10 nm)/silicon nitride (20 nm)/top TEOS oxide (20 nm) was deposited by LPCVD. Then a 150-nm-thick *in situ* n^+ doped poly-Si layer was deposited and patterned for forming the gate electrode, and the *n*-channel source and drain were doped by a self-aligned implantation with a phosphorus dosage of 5×10^{15} cm^{-2}. A 200-nm-thick LPCVD TEOS oxide layer was deposited as the passivation layer, which also served as the dopant activation anneal. Next, contact holes were opened and AlSiCu film was deposited and patterned. Finally, all devices were sintered at 400 °C in nitrogen ambient for 30 min.

A cross-sectional transmission electron microscopy (TEM) micrograph of a single nanowire channel of the NW SONOS-TFT and stacked ONO layer is shown in Fig. 1. The physical width of the nanowire channel is confirmed at 65 nm and the thickness of ONO multilayer is about 50 nm. Figure 2 presents the typical I_D-V_G curves of the SC and the proposed NW SONOS-TFTs. It is obvious that the NW device has superior performance than SC device, such as the higher on current, smaller threshold voltage (V_{th}) and subthreshold swing. The electrical parameters are also extracted in the insert tables. Since the crowding of the gate fringing field at the narrow channel surface of nanowire causes the large electrical field, the devices with nanowire structure have the better gate control ability. Hence, the device characteristics of SONOS-TFT with NW structure are mainly improved by the high electrical field originated from fringing electrical field effect.

The SONOS-TFT can also exhibit memory characteristics under adequate gate voltage operation. Because the electron injection to the nitride layer from the channel is very sensitive to the tunnel oxide thickness, the direct tunneling could almost be neglected when the thickness is thicker than 5 nm.[12,13] Therefore, in this work, the SONOS-TFT memory is programed and erased by the Fowler-Nordheim tunneling mechanism. The programing and erasing characteristics of NW and SC devices are plotted in Figs. 3(a) and 3(b). Obviously, the NW SONOS-TFT has the superior P/E efficiency due to the high electrical field. A memory window with a threshold voltage of 2.3 V shift can be achieved under a control gate bias of 15 V during 1 ms programing for the NW device. The programing speed is 1000 times of magnitude larger than that for SC device. Also, the erasing speed of NW SONOS-TFT device is about 100 times of magnitude larger than that for SC device and achieves a threshold voltage shift of −0.8 V in 10 ms erasing operation under a gate bias of −20 V. Besides the fringing electrical field effect, the corner effect induced the local tunnel current at the edges can also enhance the programing and erasing performances in memory devices with nanowire channels.[14]

Figure 4(a) shows retention characteristics of NW and SC SONOS-TFTs. The devices were programed and measured at 85 °C. It is clear that the memory window is decreased by 15% for NW SONOS-TFT and decreased by 50%

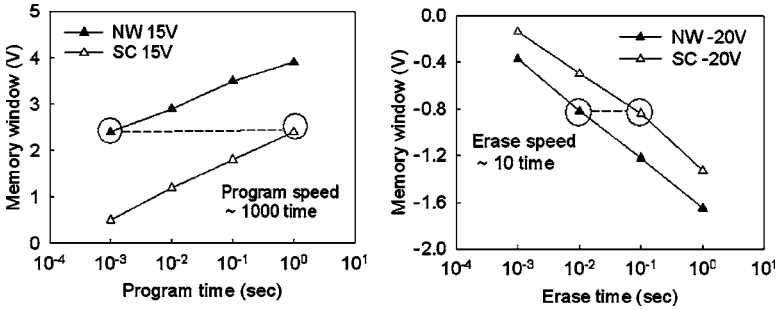

FIG. 3. (a) Programing and (b) erasing characteristics of devices for NW and SC structures.

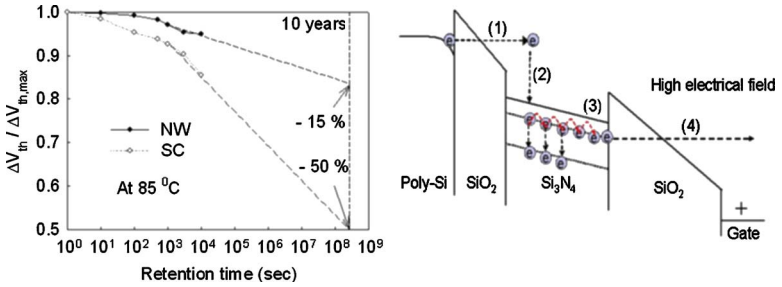

FIG. 4. (a) Retention characteristics of devices with NW and SC structures and (b) band diagram of SONOS-TFT during program operation.

for SC SONOS-TFT after extrapolating to retention time of 10 yr. This is because the threshold voltage shift is mainly contributed to the electrons trapped of the deep traps of the NW SONOS-TFT, as illustrated in Fig. 4(b). In the initial, the electrons are injected from the channel via tunneling through the tunnel oxide (path 1) during program operation. Then, the injected electrons will be captured by the traps (path 2) in the nitride (either deep traps or shallow traps). At high temperatures, some electrons captured in shallow traps can easily detrap and move to blocking oxide by the field-enhanced Poole-Frenkel emission (path 3). Finally, the detrapping electrons could inject to the gate by the large electric field (path 4). Due to the large electrical field induced by the fringing electrical field effect, most electrons trapped in the shallow traps were expulsive in NW SONOS-TFT when devices were programed at 85 °C. Hence, this lower reduction rate of ΔV_{th} could lead to longer retention time and superior reliability in the NW device.

In summary, we have demonstrated the poly-Si TFT consisted of oxide/nitride/oxide stack gate dielectric and multiple nanowire channels. Experimental results show that the electrical characteristics of poly-Si TFT devices are enhanced as channel width decreases from 1 μm (SC structure) to 65 nm (NW structure). The NW poly-Si TFT devices have the superior gate controllability due to the fringing electrical field effect induced high electrical field. In addition, the proposed NW SONOS-TFT exhibits superior memory device characteristics with high program/erase efficiency and stable retention characteristics. The fabrication of SONOS-TFTs with nanowire channels is quite easy and involves no additional processes. Such a SONOS-TFT is thereby highly promising for application in the future system-on-panel display applications.

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